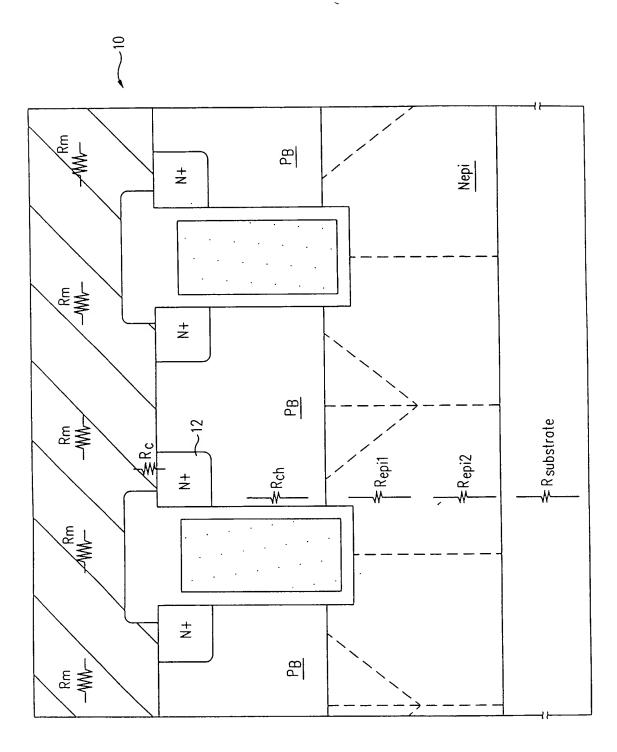


(PRIOR ART) FIG. 1



(PRIOR ART) FIG. 2

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 3 of 58

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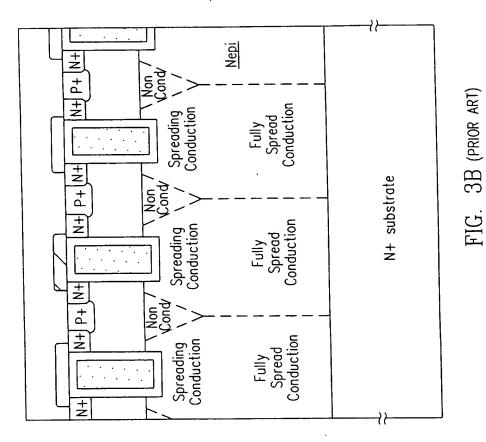
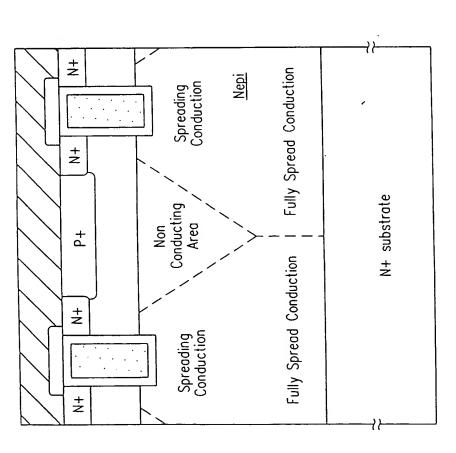
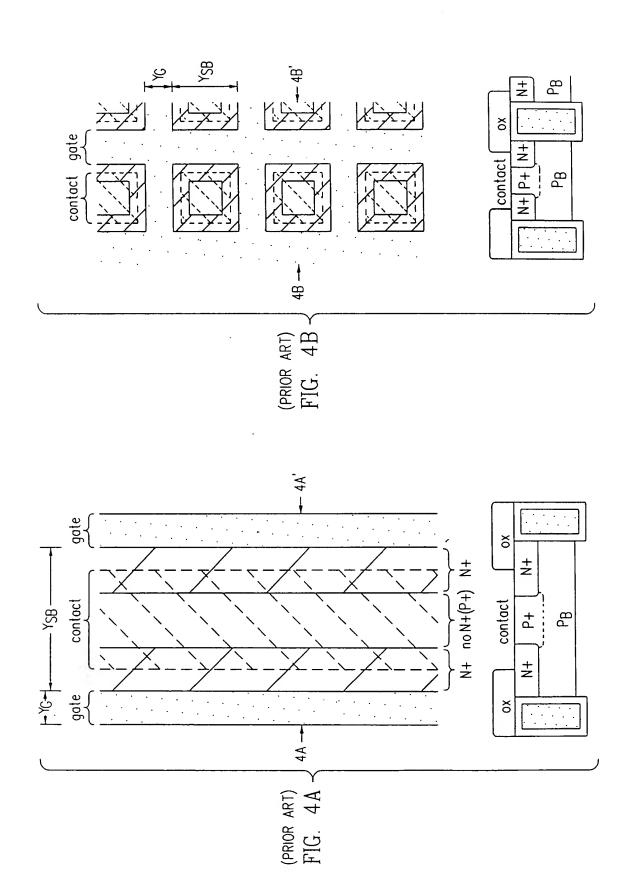


FIG. 3A (PRIOR ART)

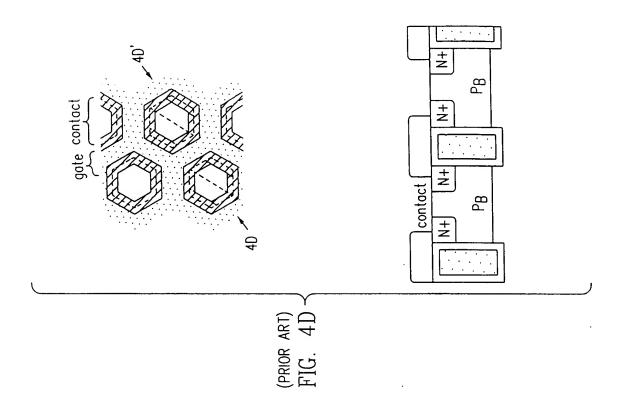


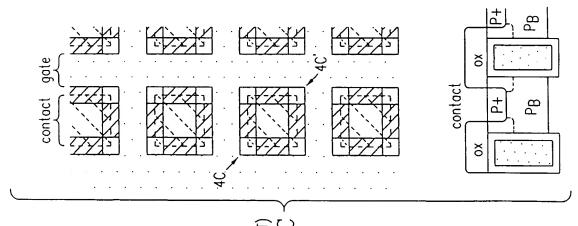
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 4 of 58



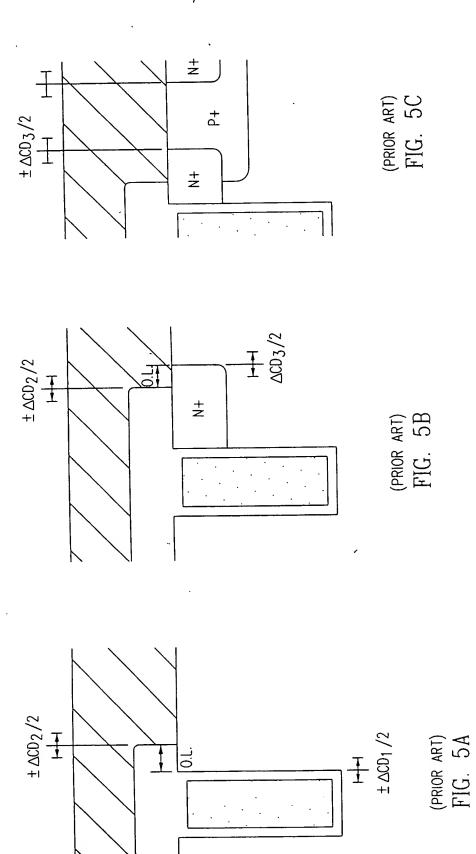
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 5 of 58

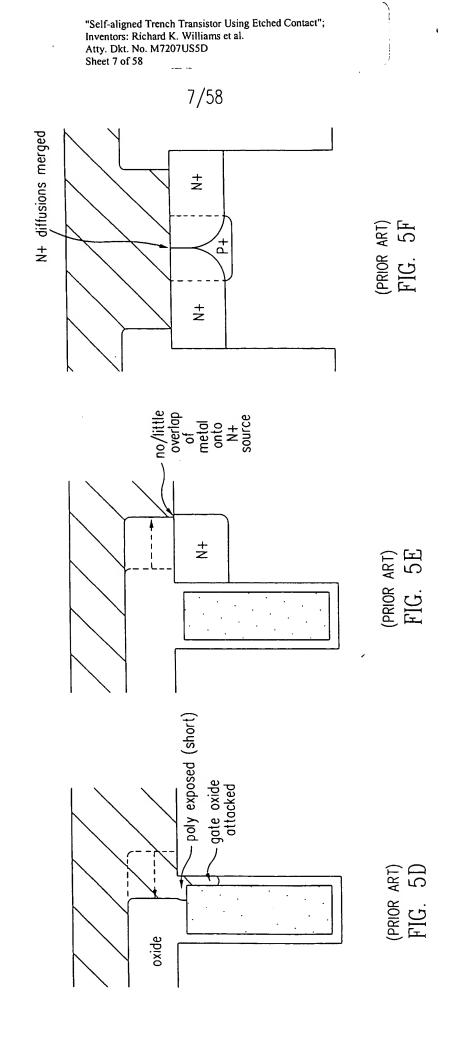
5/58



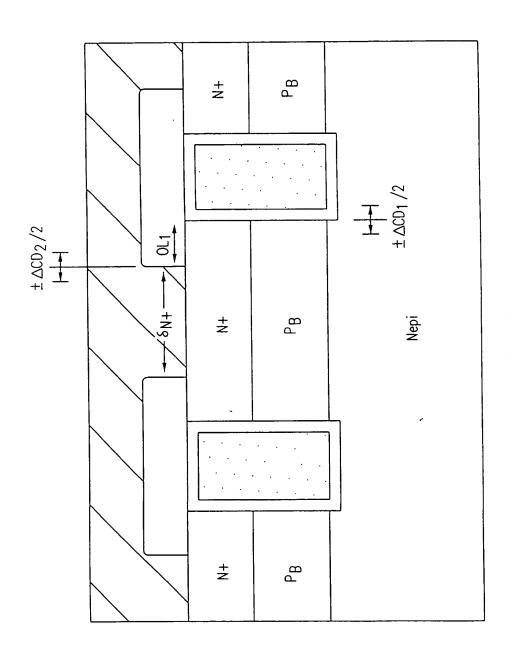


(PRIOR ART) FIG. 4C <





"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 8 of 58

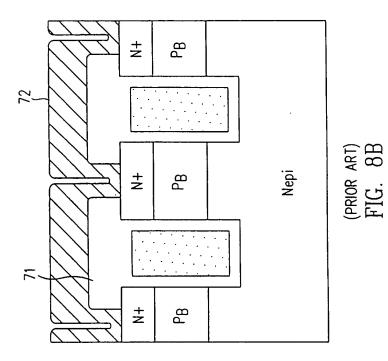


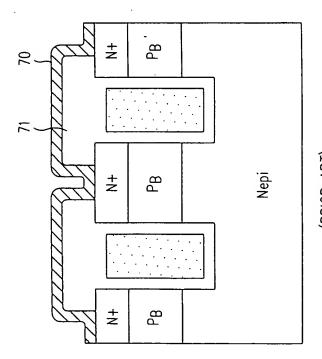
(PRIOR ART) FIG. 6

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 9 of 58 9/58 (PRIOR ART) FIG. 7B z direction (PRIOR ART) FIG. 7C 4 РВ z direction Рв ż N+ substrate (PRIOR ART) FIG. 7A ·Nepi РВ ŧ ŧ Рв

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 10 of 58

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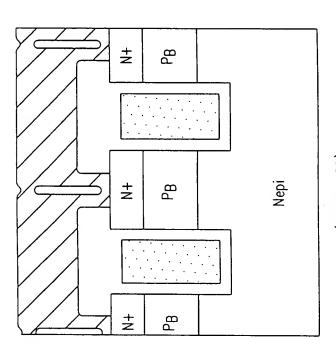




(PRIOR ART) FIG. 8A

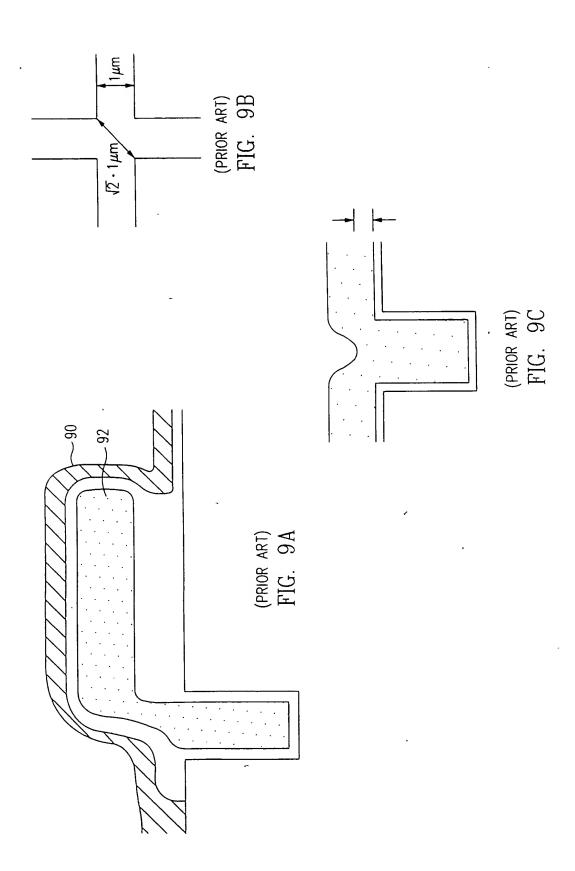
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 11 of 58

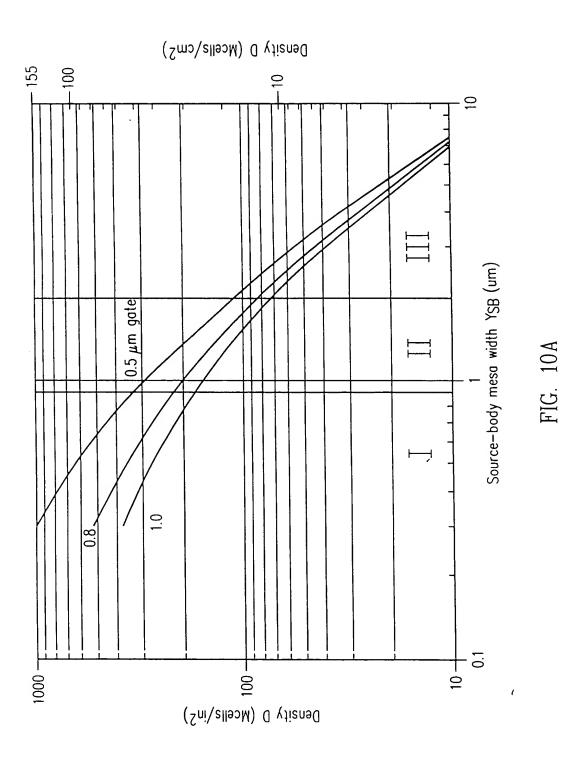
11/58

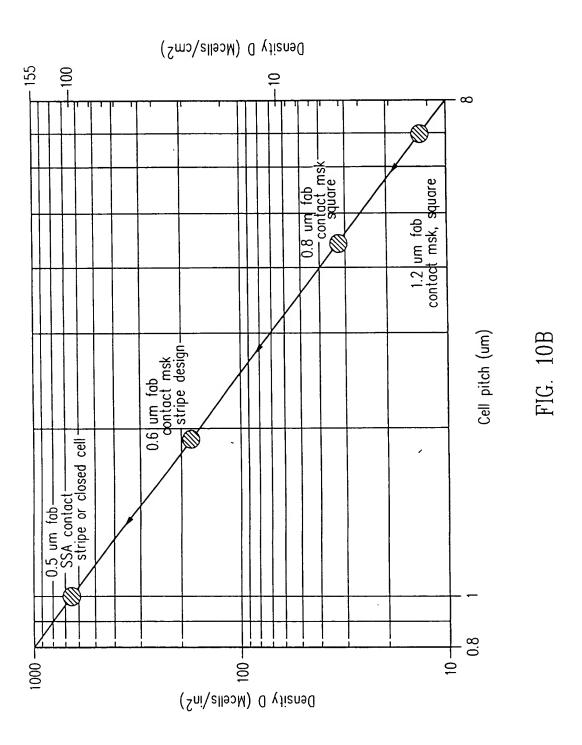


(PRIOR ART) FIG. 8C

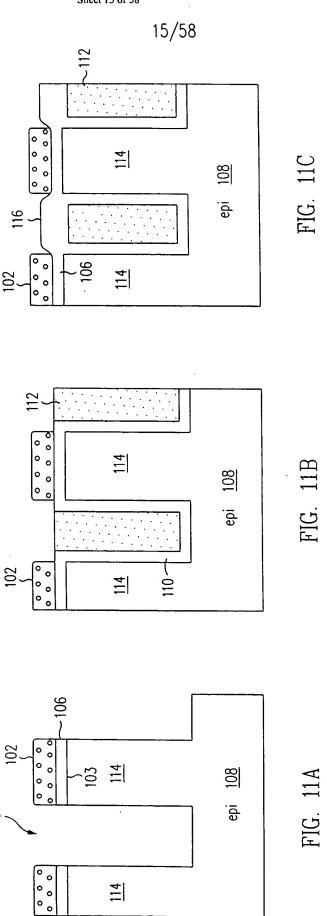
12/58



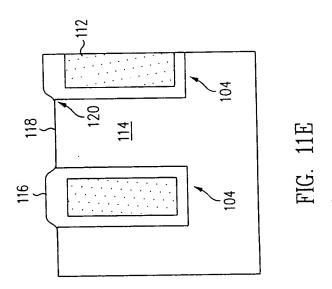


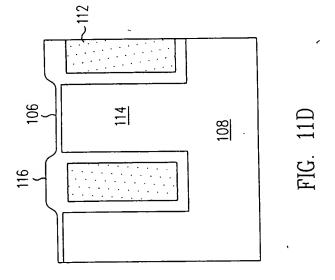


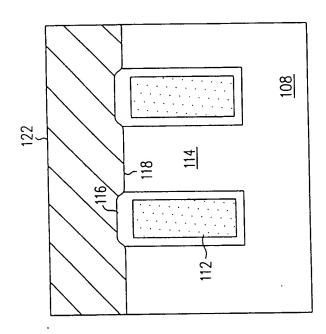
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 15 of 58



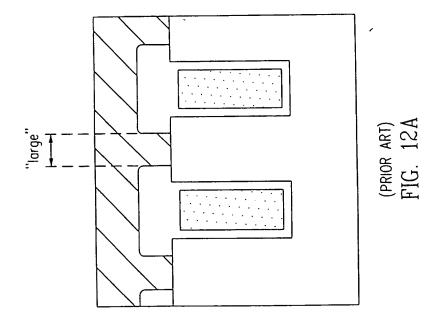
16/58



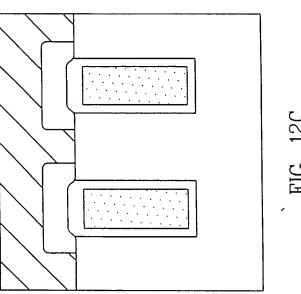


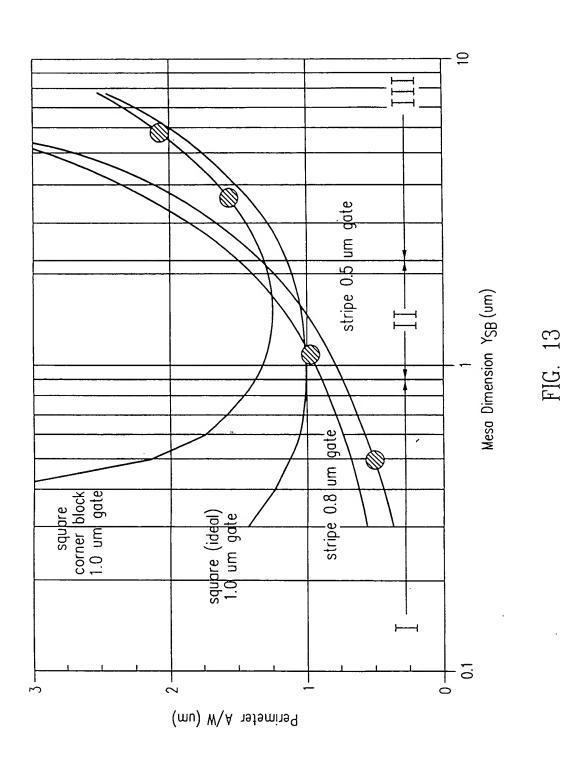


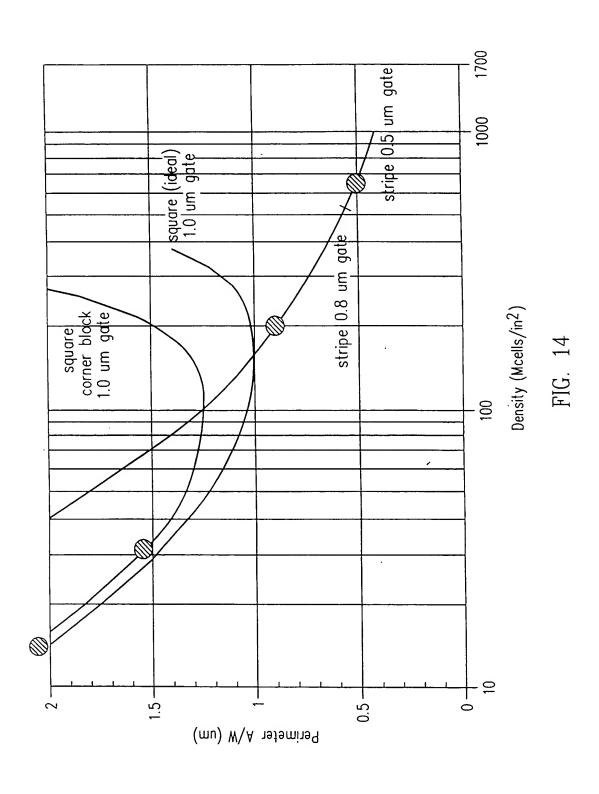
7G. 12B



"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 18 of 58







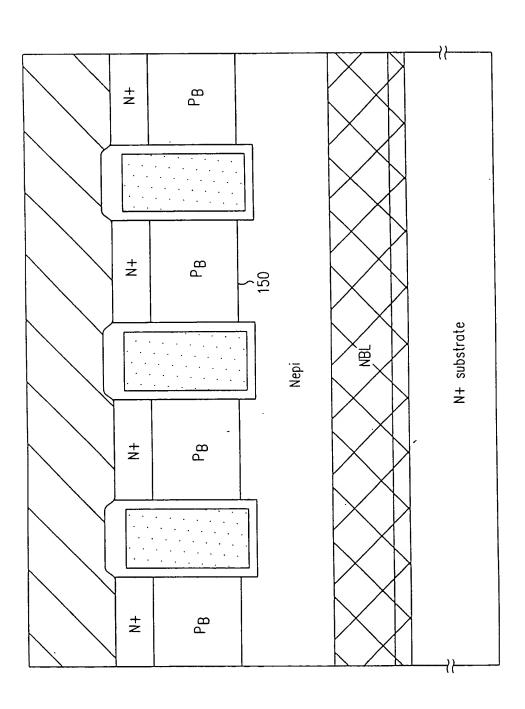
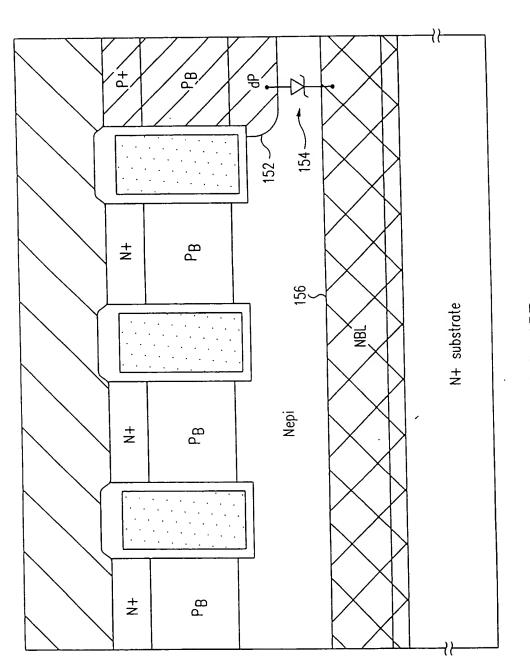


FIG. 15A

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 22 of 58



"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 23 of 58

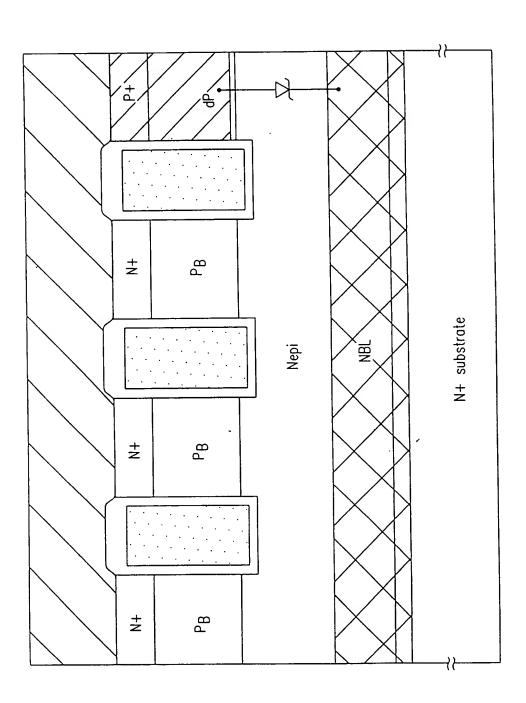


FIG. 15C

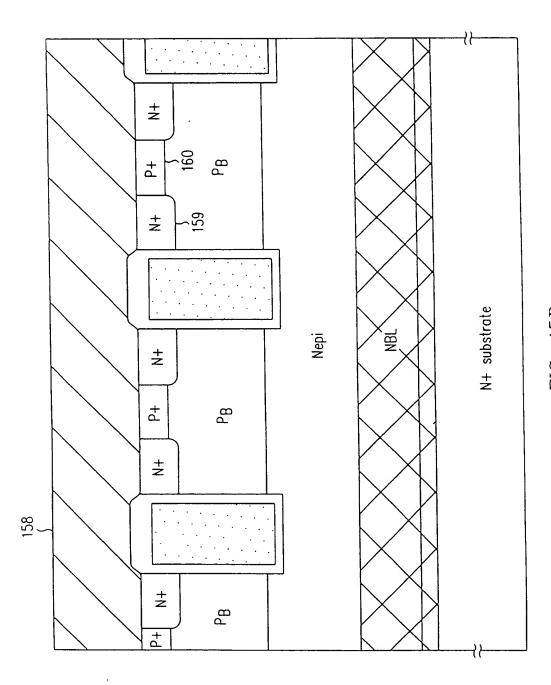
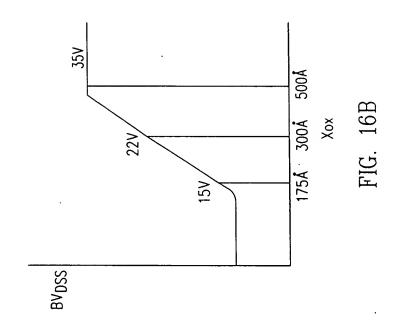
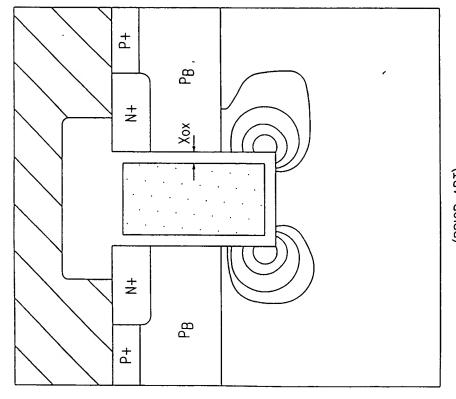


FIG. 15D

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 25 of 58

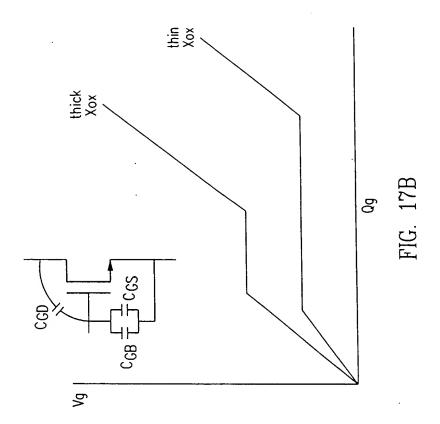




(PRIOR ART) FIG. 16A

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 26 of 58

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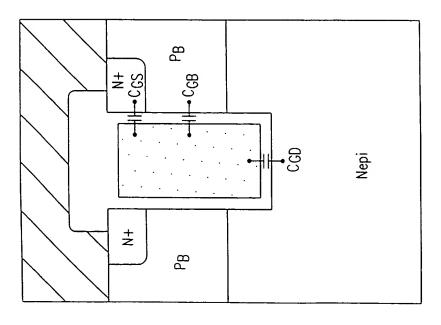


FIG. 17A

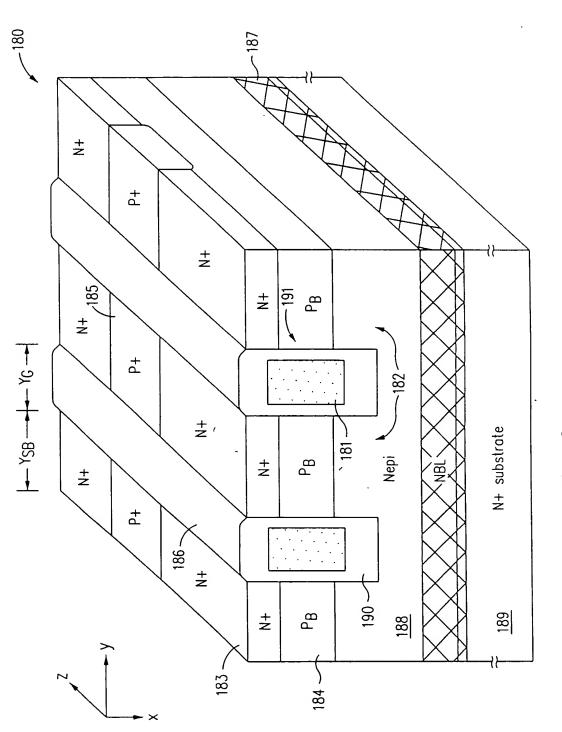
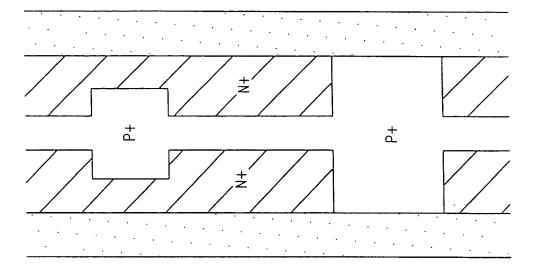
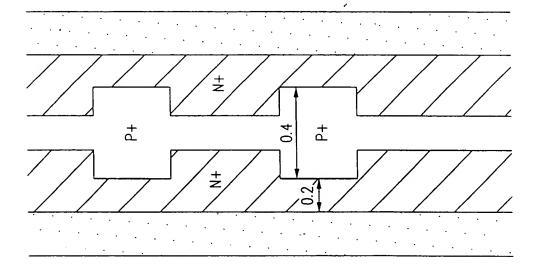
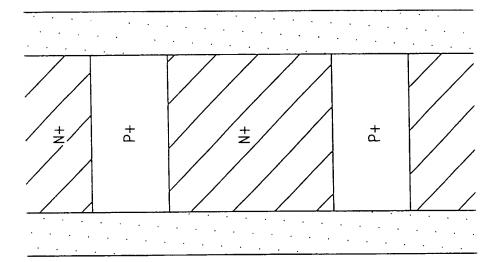


FIG. 18

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 28 of 58







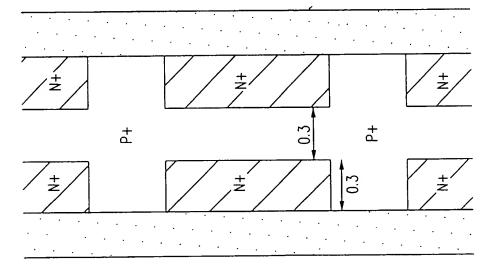
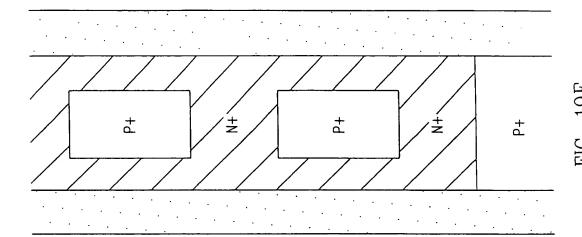


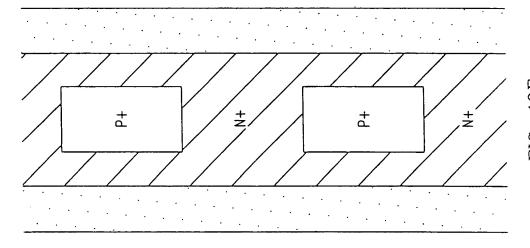
FIG 19D

FIG. 19C

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 30 of 58

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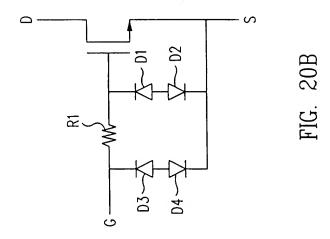


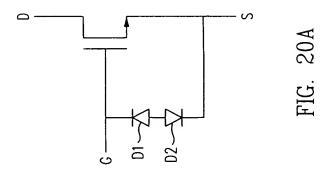


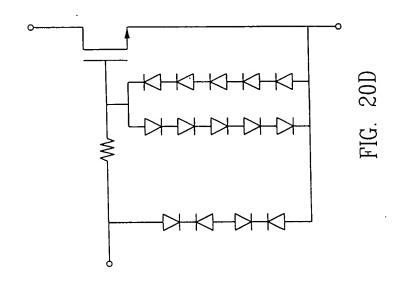
<u> Я</u>6]

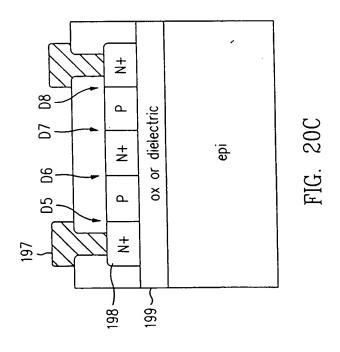
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207USSD Sheet 31 of 58

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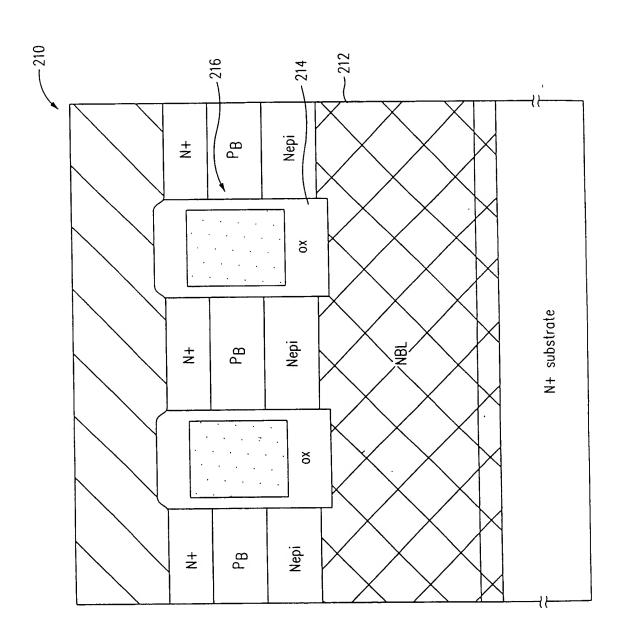








"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 33 of 58



7IG. 21

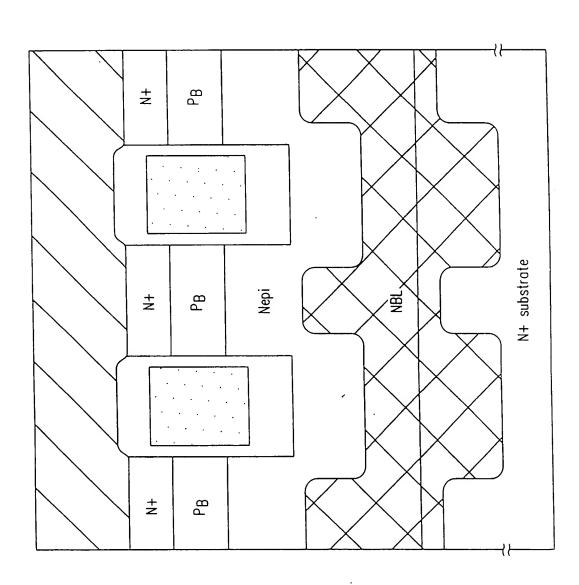


FIG. 211

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 35 of 58

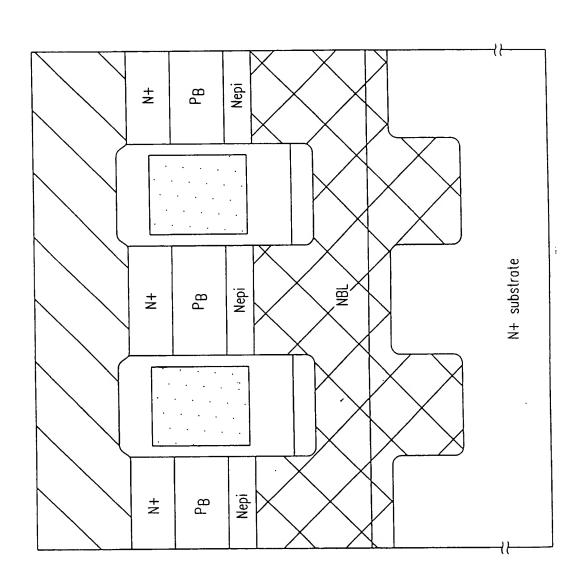


FIG. 22

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 37 of 58

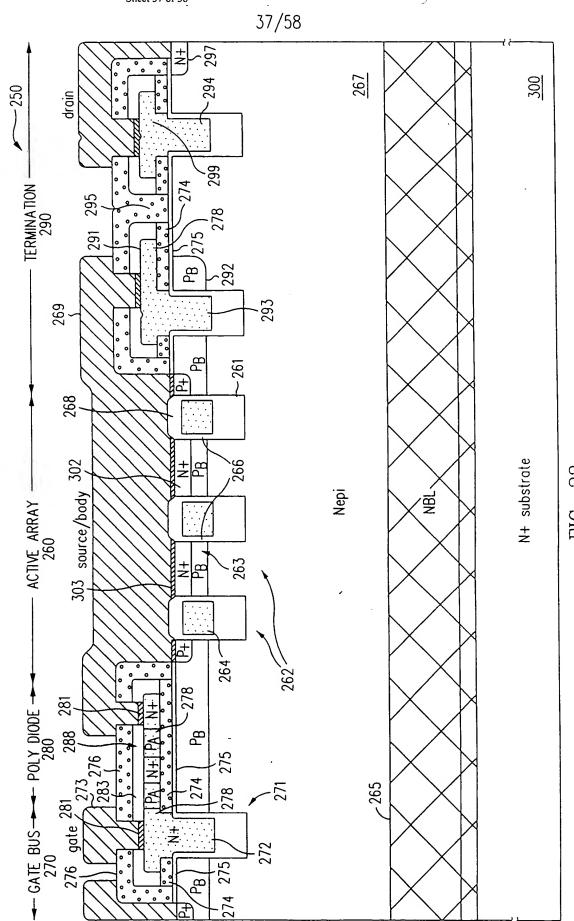


FIG. 23

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 38 of 58

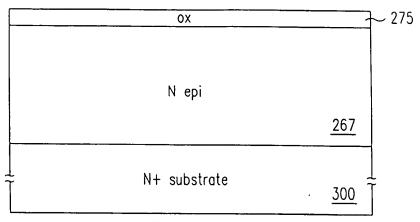


FIG. 24A

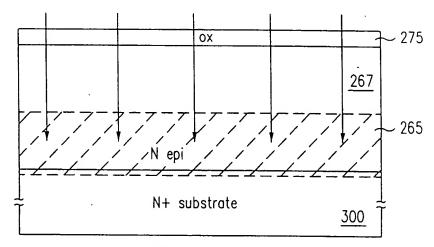


FIG. 24B

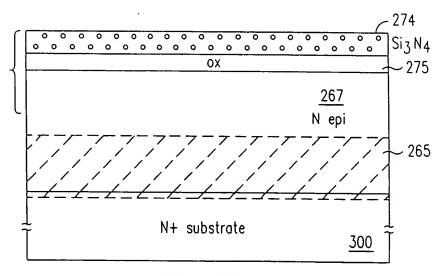


FIG. 24C

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 39 of 58

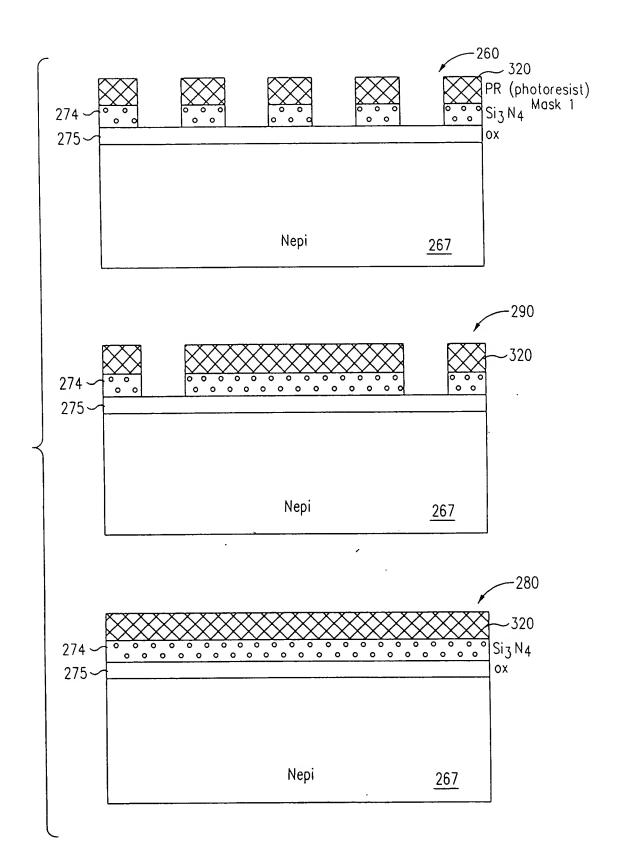


FIG. 24D

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 40 of 58

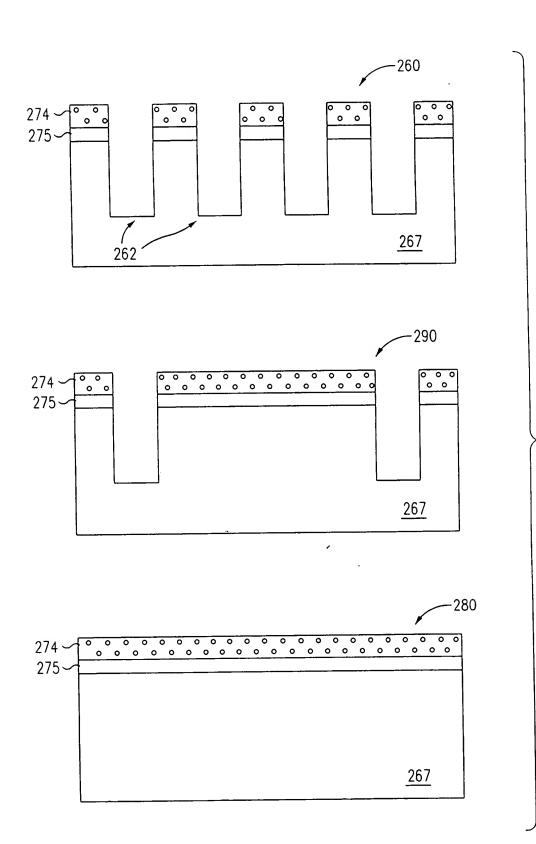


FIG. 24E

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 41 of 58

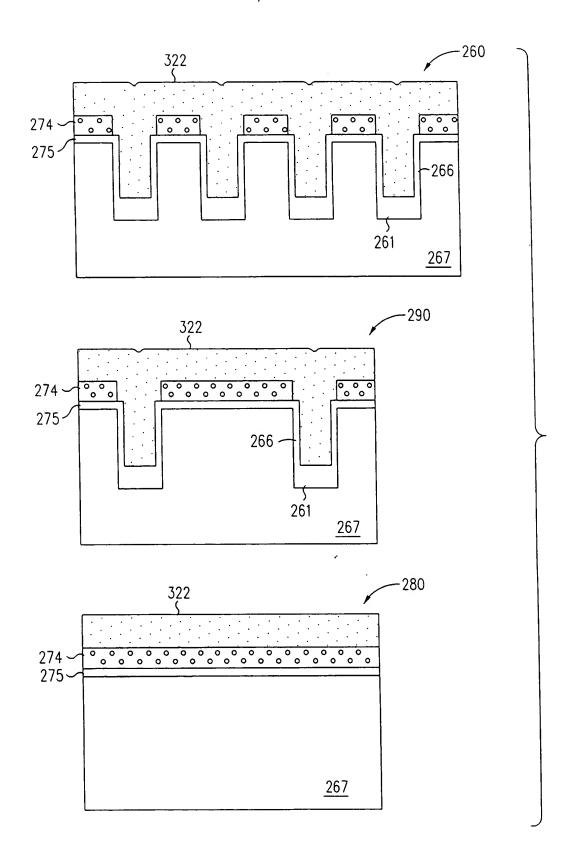


FIG. 24F

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 42 of 58

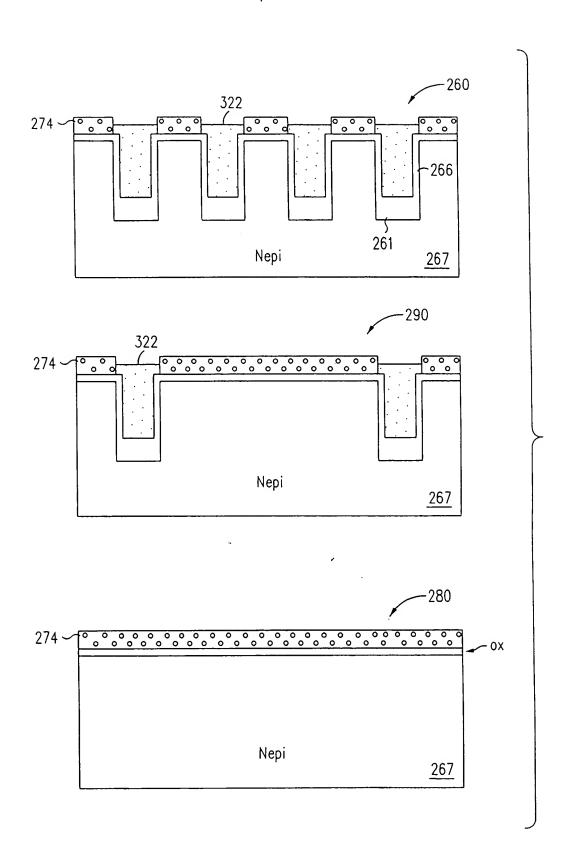


FIG. 24G

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 43 of 58

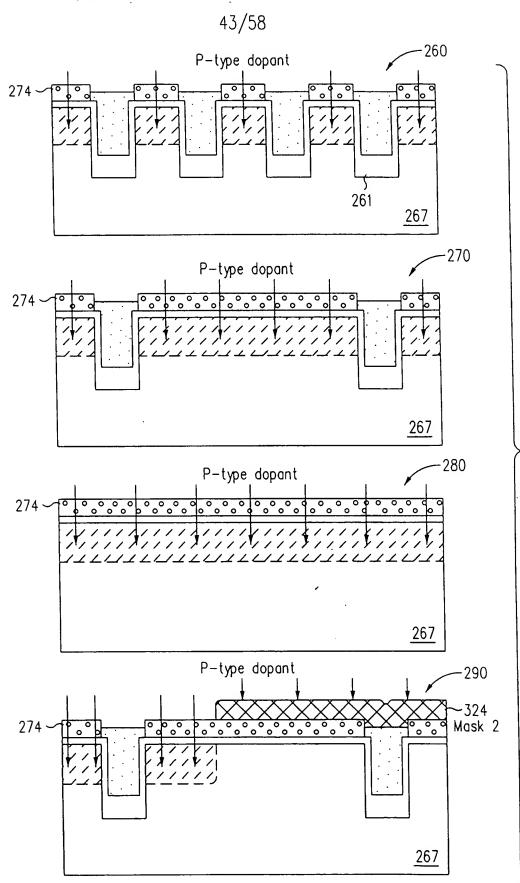


FIG. 24H

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 44 of 58_

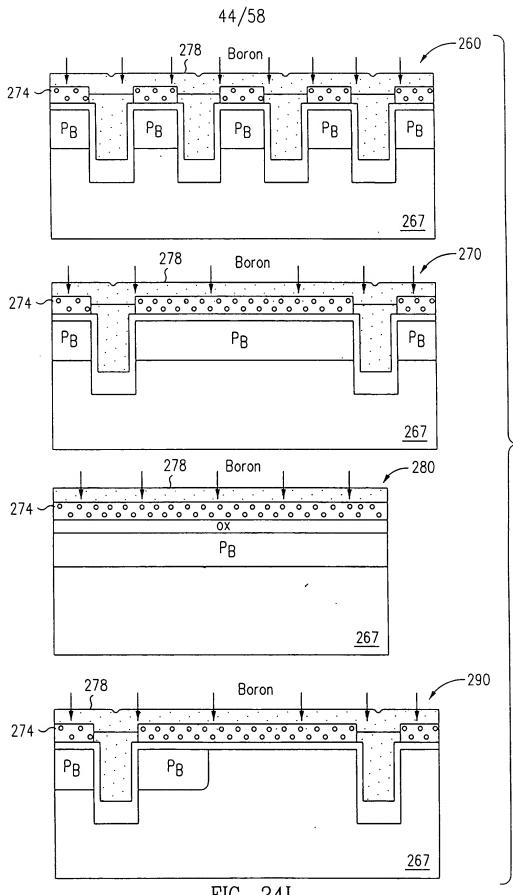


FIG. 24I

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 45 of 58

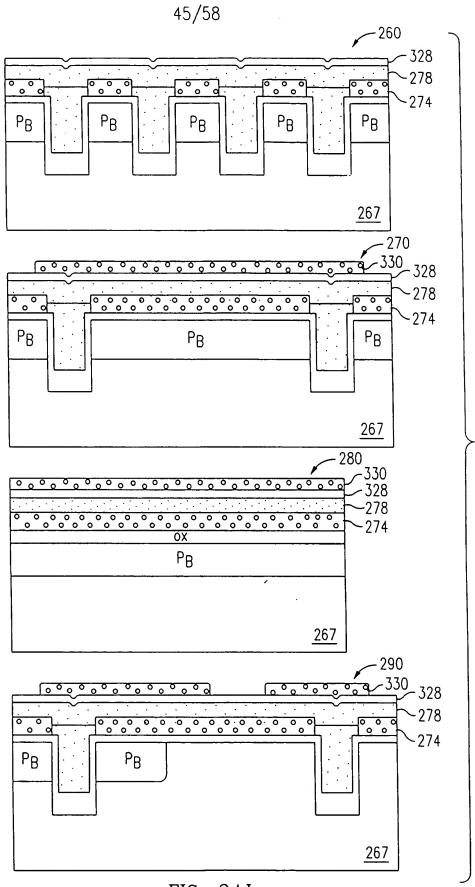


FIG. 24J

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 46 of 58

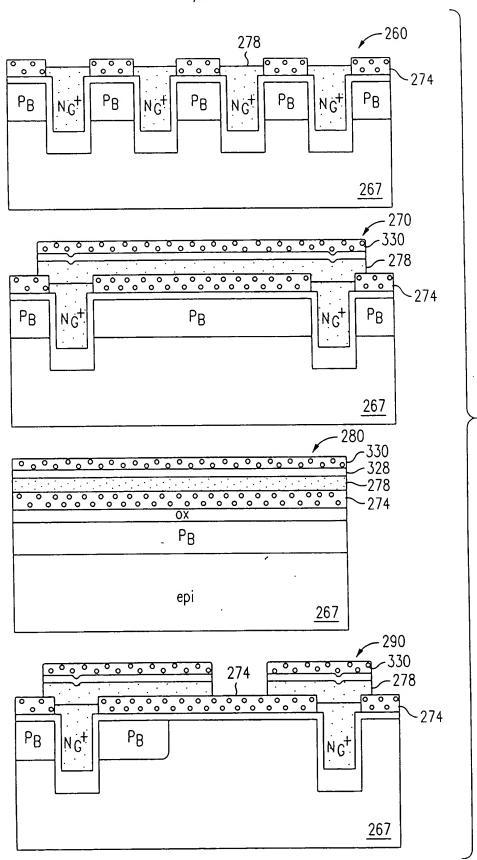


FIG. 24K

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 47 of 58

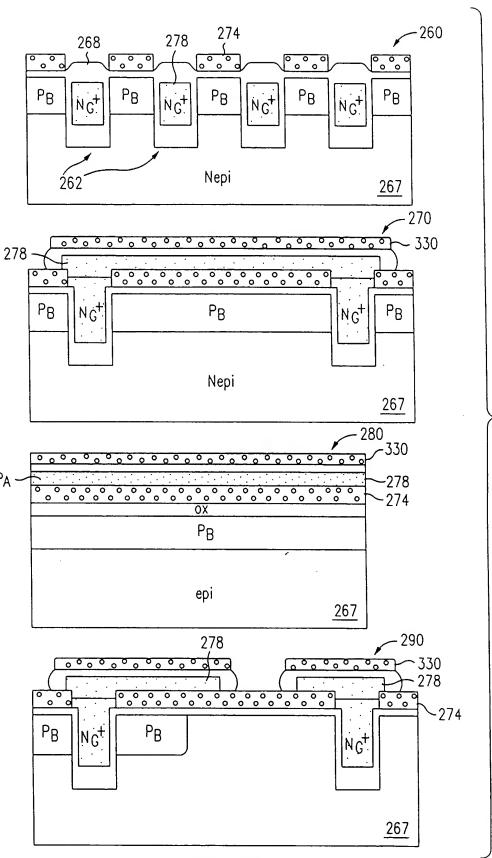


FIG. 24L

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 48 of 58



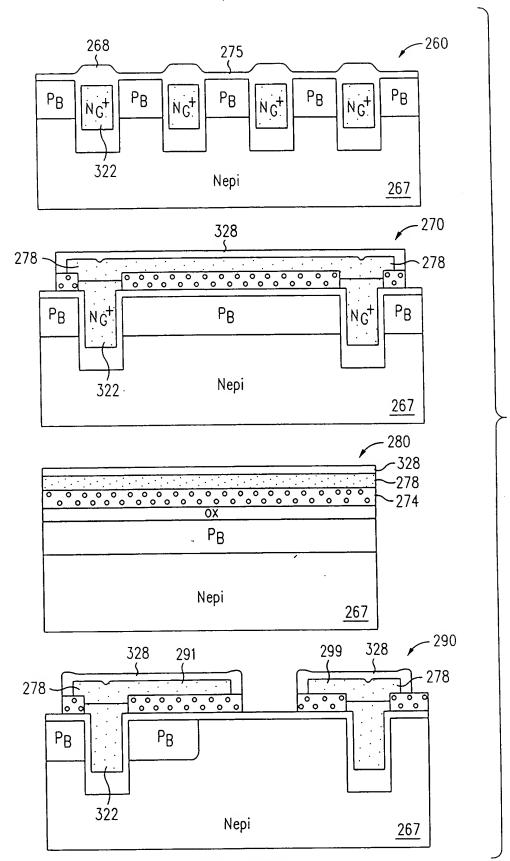


FIG. 24M

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 49 of 58

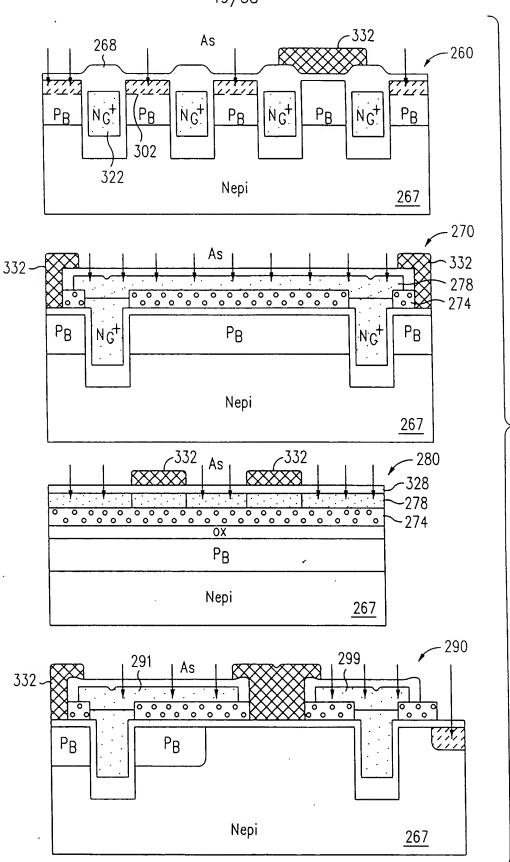


FIG. 24N

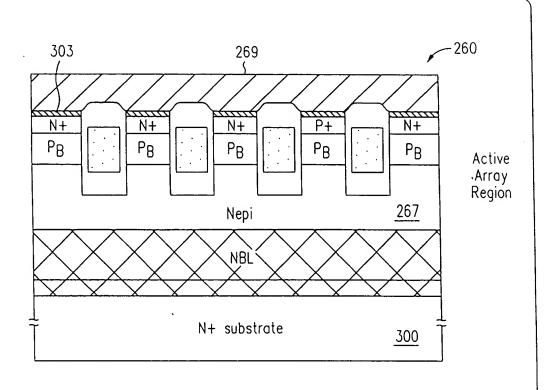
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 50 of 58 50/58 BF₂ 260 N+ NG+ PΒ NG^{\dagger} NG+ PΒ Active PB PB PB Array Región Nepi <u> 267</u> 270 328 276 278 Gate РΒ PB Bus NG+ PB Region Nepi 267 280 BF₂ BF₂ 328 276 278 Poly Diode P_{B} Region Nepi <u> 267</u> 290 276 278 **Termination** Region N+ РΒ PB NG^{+} NG

FIG. 240

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Nepi

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 51 of 58



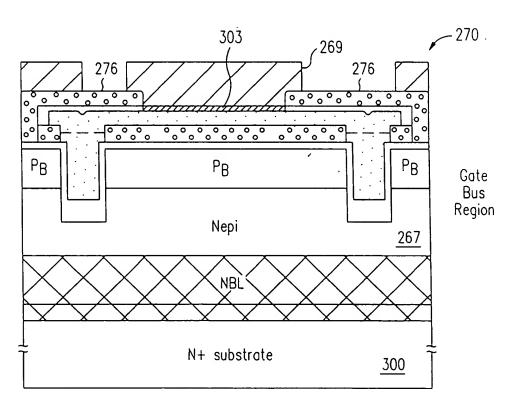
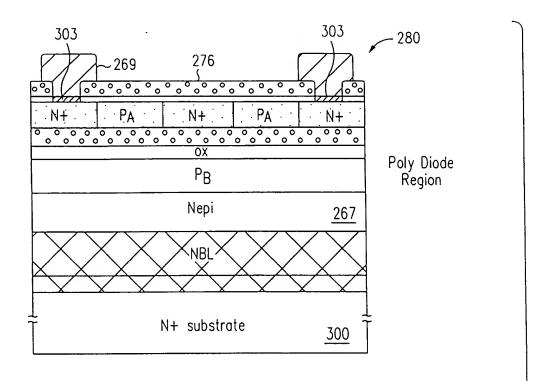


FIG. 24P

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207USSD Sheet 52 of 58



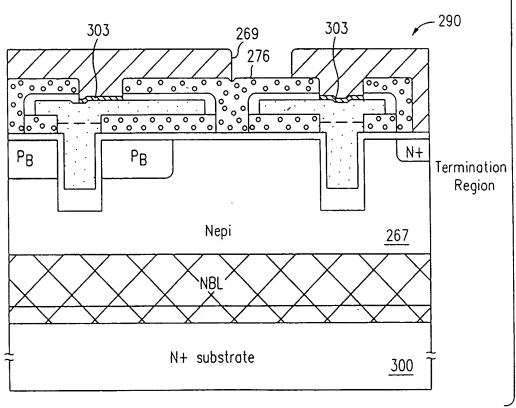
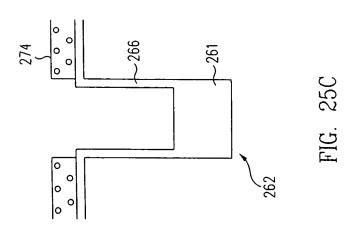
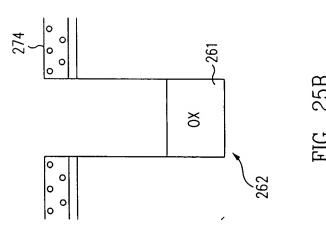
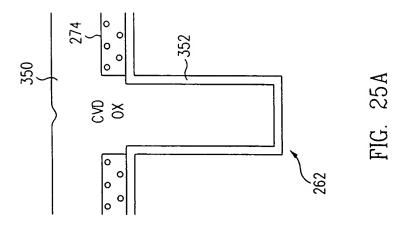


FIG. 24Q



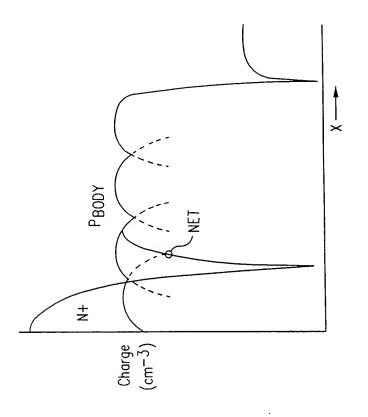






"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 54 of 58

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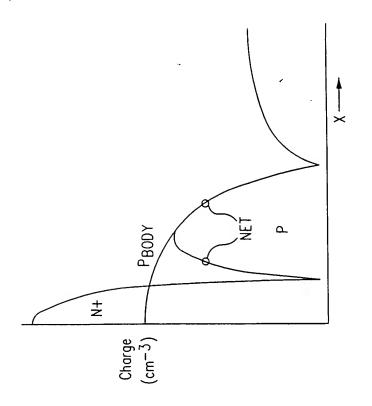


FIG. 26A

FIG. 26B

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 55 of 58

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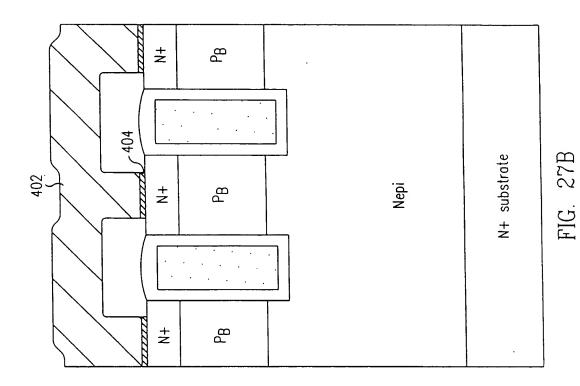
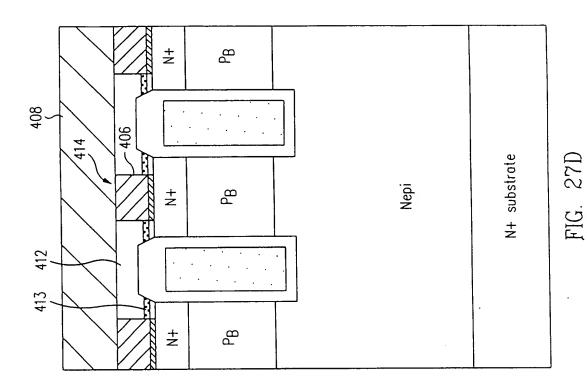


FIG. 27A



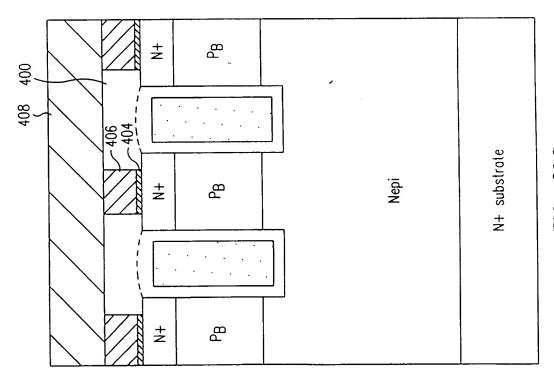


FIG. 27C

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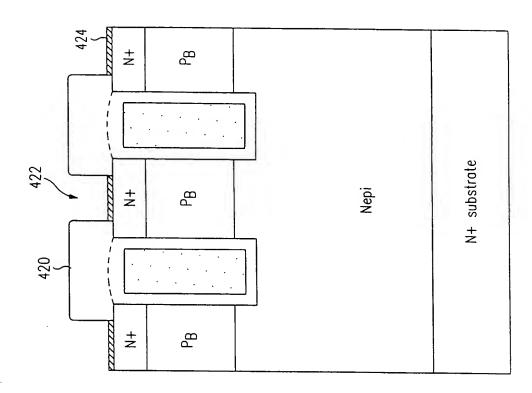


FIG. 28B

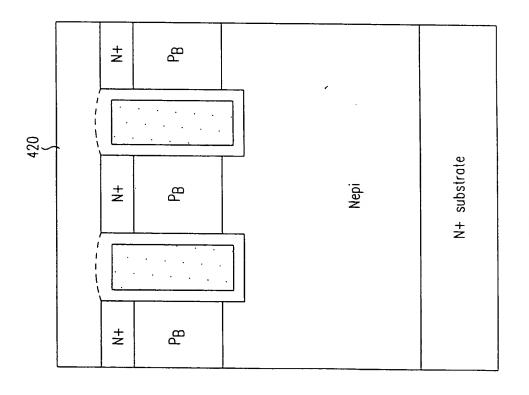


FIG. 28A

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207USSD Sheet 58 of 58

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